REMARKS

Claims 1-115 are pending. In this Response, claims 111-115 have been added.

I. RESTRICTION REQUIREMENT

A Petition for Withdrawal of Restriction Requirement is filed herewith.

The Examiner asserts that "A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR § 1.144 & MPEP § 821.01)." This is clearly erroneous. The outstanding Office Action is not final. Furthermore, the Petition for Withdrawal of Restriction Requirement is pending. Therefore, Applicant requests that the requirement for "cancellation of non-elected claims or other appropriate action" be withdrawn.

II. SPECIFICATION CORRECTION

The Examiner requests Applicant's cooperation in correcting any errors of which Applicant may be aware in the Specification. Applicant is not aware of any errors in the Specification.

III. SPECIFICATION ADVICE

The Examiner advises that "The use of the trademark Enthone Enplate NI-424 on page 34, line 25 or any others has been noted in this application. It should be capitalized whenever it appears and be accompanied by the generic terminology." Applicant acknowledges the advice.

IV. SPECIFICATION OBJECTION

The Specification is objected to because Applicant's related applications information should be updated. The Specification has been amended in this manner. Therefore, Applicant requests that the Specification objection be withdrawn.

V. DRAWING OBJECTIONS

The drawings are objected to under 37 C.F.R. § 1.83(a) since the drawings must show every feature of the invention specified in the claims, and therefore various features must be shown or canceled from the claims.

The Examiner asserts that the drawings must show "the connection joint includes a nickel layer and a gold layer, the nickel layer contacts the routing line and the pad, and the gold layer is spaced from the routing line and the pad in claims 25 and 37."

Claimed features need not necessarily be shown in the drawings, as is clear from the many patents that issue without drawings:

> The applicant shall furnish a drawing where necessary for the understanding of the subject matter sought to be patented. When the nature of such subject matter admits of illustration by a drawing and the applicant has not furnished such a drawing, the Commissioner may require its submission within a time period of not less than two months from sending a notice thereof. (35 U.S.C. § 113.)

The Specification illustrates connection joint 170 as follows:

> **FIGS. 17A, 17B** and **17C** are cross-sectional, top and bottom views, respectively, of connection joint 170 formed on pad 116 and routing line 132 . . . (Page 34, lines 1-2.)
>
> More particularly, connection joint 170 is plated on pad 116 and elongated region 134 of routing line 132 in through-hole 166 . . . during an electroless plating operation. (Page 34, lines 6-9.)
>
> Connection joint 170 is composed of a nickel layer electrolessly plated on pad 116 and routing line 132 and a gold layer electrolessly plated on the nickel layer . . . In connection joint 170, the nickel layer contacts and is sandwiched between pad 116 and the gold layer and between routing line 132 and the gold layer, and the gold layer is spaced and separated from pad 116 and routing line 132 and exposed . . . For convenience of illustration, the nickel and gold layers are shown as a single layer. (Page 34, lines 10-24.)

The structure is submerged in an electroless nickel plating solution . . . (Page 34, line 24.)

Pad 116 includes an exposed nickel surface layer and therefore is catalytic to electroless nickel. . . . As a result, connection joint 170 begins to plate on pad 116. However, connection joint 170 does not initially deposit on routing line 132 . . . In other words, the exposed portions of conductive trace 152 are copper which is not catalytic to electroless nickel. (Page 35, lines 14-23.)

As the electroless nickel plating operation continues, connection joint 170 continues to plate on pad 116 and expand vertically in through-hole 166 towards routing line 132. Eventually connection joint 170 contacts routing line 132 in through-hole 166 and changes the electrochemical potential of routing line 132 by a small amount such as 0.2 volts. . . As a result, routing line 132 . . . become[s] catalytic to electroless nickel, [and] connection joint 170 begins to plate on routing line 132 as well . . . (Page 35, line 24 to page 36, line 1.)

The electroless nickel plating operation continues until connection joint 170 is about 15 microns thick. (Page 36, lines 3-4.)

Thereafter, the assembly is removed from the electroless nickel plating solution and briefly submerged in an electroless gold plating solution such as is MacDermid PLANAR™ at 70°C. Connection joint 170 . . . include[s] an exposed nickel surface [layer] and therefore [is] catalytic to electroless gold. . . . As a result, the gold deposits on the nickel surface [layer]. The gold electroless plating operation continues until the gold surface [layer is] about 0.5 microns thick. Thereafter, the structure is removed from the electroless gold plating solution and rinsed in distilled water. (Page 36, lines 8-16.)

Connection joint 170 includes a buried nickel layer and a gold surface layer. The buried nickel layer provides the primary mechanical and electrical connection between pad 116 and routing line 132, and the gold surface layer is a relatively unimportant byproduct of the electroless plating operation. (Page 36, lines 24-27.)

> **FIGS. 17D, 17E** and **17F** are enlarged cross-sectional, bottom and cross-sectional views, respectively, of connection joint 170. FIG. 17F is oriented orthogonally with respect to FIG. 17D. As is seen, connection joint 170 extends into through-hole 166 and contacts and electrically connects pad 116 and routing line 132. Furthermore, connection joint 170 contacts the downwardly facing surface and elongated peripheral sidewalls of routing line 132, and adhesive 154 remains in contact with and sandwiched between pad 116 and routing line 132. (Page 37, line 25 to page 38, line 2.)

Figs. 17A and 17D-17F and the related text make abundantly clear that connection joint 170 includes a buried nickel layer that contacts routing line 132 and pad 116 and an exposed surface gold layer that contacts the nickel layer and is spaced from routing line 132 and pad 116. An additional figure such as a cross-sectional view similar to Fig. 17D that shows the boundary between the nickel layer and the gold layer would be redundant and unenlightening and unnecessarily clutter the captioned-application with another figure to show a feature that is apparent to those skilled in the art.

The Examiner also asserts that the drawings must show "the first and second surfaces of the pillar have a circular shape in claim 106; the first surface of the pillar is concentrically disposed within a surface area of the second surface of the pillar in claim 107; the pillar is copper and has a conical shape, the first and second surfaces of the pillar are flat and parallel to one another and have a circular shape, and the first surface of the pillar is concentrically disposed within a surface area of the second surface of the pillar in claim 110."

The Specification illustrates pillar 144 as follows:

> **FIGS. 8A, 8B** and **8C** are cross-sectional, top and bottom views, respectively, of pillar 144 formed from metal base 120. (Page 22, lines 3-4.)
>
> Pillar 144 is formed by applying a wet chemical etch to metal base 120 using etch mask 130 to selectively protect metal base 120. Thus, pillar 144 is an unetched portion of metal base 120 defined by etch mask 130 that is formed subtractively. (Page 22, lines 5-7.)

The wet chemical etch laterally undercuts metal base 120 beneath etch mask 130, causing pillar 144 to taper inwardly with increasing height. A suitable taper is between 45 and slightly less than 90 degrees, such as approximately 75 degrees. (Page 22, lines 27-29.)

Pillar 144 includes opposing surfaces 146 and 148 and tapered sidewalls 150 therebetween. Surface 146 of pillar 144 constitutes an unetched portion of surface 122 of metal base 120, and surface 148 of pillar 144 constitutes an unetched portion of surface 124 of metal base 120. Surface 146 contacts and faces towards etch mask 130 and is spaced from and faces away from routing line 132, and surface 148 contacts and faces towards routing line 132 and is spaced from and faces away from etch mask 130. Surfaces 146 and 148 are flat and parallel to one another. Tapered sidewalls 150 are adjacent to surfaces 146 and 148 and slant inwardly towards surface 146. (Page 23, lines 13-20.)

Pillar 144 has a conical shape with a height (between surfaces 146 and 148) of 250 microns and a diameter that decreases as the height increases (towards surface 146 and away from surface 148). Surface 146 has a circular shape with a diameter of 300 microns, and surface 148 has a circular shape with a diameter of 500 microns. Thus, surface 146 has a surface area of 70,650 square microns ($\pi(300/2)^2$), and surface 148 has a surface area of 196,250 square microns ($\pi(500/2)^2$). Accordingly, the surface area of surface 146 is 36 percent as large as the surface area of surface 148. In other words, the surface area of surface 146 is 64 percent smaller than the surface area of surface 148 ((196,250–70,650)/196,250). (Page 23, lines 21-29.)

Surfaces 146 and 148 are vertically aligned with etch mask 130, with enlarged circular region 136, and with one another. Thus, surface 146 is concentrically disposed within the surface areas of etch mask 130, enlarged circular region 136 and surface 148, and the periphery of surface 146 is laterally offset from the peripheries of etch mask 130, enlarged circular region 136 and surface 148 by 100 microns ((500–300)/2). (Page 24, lines 1-5.)

The Specification also illustrates pillar 144 in Figs. 9A-9B, 10A-10B and 11A-11B after etch mask 130 is removed.

Figs. 8A, 9A-9B, 10A-10B and 11A-11B and the related text make abundantly clear that first surface 146 and second surface 148 of pillar 144 have a circular shape (claim 106), first surface 146 of pillar 144 is concentrically disposed within a surface area of second surface 148 of pillar 144 (claim 107), pillar 144 has a conical shape, first surface 146 and second surface 148 of pillar 144 are flat and parallel to one another and have a circular shape, and first surface 146 of pillar 144 is concentrically disposed within a surface area of second surface 148 of pillar 144 (claim 110).

If the Examiner persists in the objection that the drawings must show "the pillar is copper," perhaps the Examiner can enlighten Applicant as to how the drawings can illustrate the pillar is copper as opposed to gold, aluminum or another metal.

Therefore, Applicant requests that these objections be withdrawn.

VII. SECOND 112, SECOND PARAGRAPH REJECTIONS

Claims 25, 37, 40, 41, 43, 44, 46, 48, 50-52, 54-58, 61, 62, 64, 66-68 and 101-110 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Examiner asserts that "In claims 25 and 37, it is unclear and confusing to what is meant by 'the connection joint includes a nickel layer and a gold layer, the nickel layer contacts the routing line and the pad, and the gold layer is spaced from the routing line and the pad.' Where is the multiple layered structure shown? Where is this shown in the drawings of the elected species of figures 19A-19C?"

The limitations are clear and straightforward. Furthermore, the limitations need not be illustrated in the Drawings, as mentioned above. Unfortunately, the Examiner has not even attempted to explain what is unclear or confusing about these limitations. Moreover, Claim 37 does not recite these limitations.

The Examiner also asserts that "In claim 40, it is unclear and confusing to what is meant by 'the assembly is devoid of wire bonds and TAB leads.' Where is this shown in the drawings of the elected species of figures 19A-19C?"

This claim recites a negative limitation. Namely, the assembly has no wire bonds and has no TAB leads. The M.P.E.P. sanctions negative limitations as follows:

> The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection sought are set forth definitely, albeit negatively, the claim complies with the requirements of 35 U.S.C. 112, second paragraph. (M.P.E.P. § 2173.05(i).)

The Examiner's attempt to preclude Applicant from pursuing negative limitations under the guise that the negative limitations are not shown in the drawings is illogical and improper. This approach would abolish negative limitation practice.

Furthermore, numerous U.S. patents include this negative limitation in the claims without illustrating this negative limitation in the drawings. See, for instance, U.S. Patent Nos. 6,544,813; 6,548,393; 6,562,709; 6,576,539; 6,653,217; 6,660,626; 6,667,229; 6,673,710; 6,716,670 and 6,744,126. Examiners Berry, Clark, Dang, Lebentritt, Picardat, Richards and Rocchegiani had no problem allowing this negative limitation in these patents without illustrating this negative limitation in the drawings.

If the Examiner persists in this objection, perhaps the Examiner can enlighten Applicant as to how the drawings can illustrate the absence of wire bonds and TAB leads.

The Examiner also asserts that "In claims 41 and 61, it is unclear and confusing to what is meant by 'the first surface of the pillar faces away from and is spaced from the routing line.' Where is this shown in the drawings of the elected species of figures 19A-19C?"

The limitations are clear and straightforward. Furthermore, the limitations are illustrated in the Drawings. For instance, Figs. 8A, 9A-9B, 10A-10B and 11A-11B make abundantly clear that first surface 146 of pillar 144 faces away from and is spaced from routing line 132.

Unfortunately, the Examiner has not even attempted to explain what is unclear or confusing about these limitations.

The Examiner also asserts that "In claims 101 to 110, the dependency of these claims which can be depending on (possibly 41, 61) 71, 81 and 91 is confusing since the elected species does not include these independent claims.

Claims 101-110 need not be amended to exclude non-elected claims 71, 81 and 91 since these claims are pending. Furthermore, a Petition for Withdrawal of Restriction Requirement is filed herewith, as mentioned above.

The Examiner also asserts that "In claim 106, it is unclear and confusing to what is meant by 'the first and second surfaces of the pillar have a circular shape.' Where is this shown in the drawings of the elected species of figures 19A-19C?"

The limitations are clear and straightforward. Furthermore, the limitations are illustrated in the Drawings, as mentioned above. Unfortunately, the Examiner has not even attempted to explain what is unclear or confusing about these limitations.

The Examiner also asserts that "In claim 107, it is unclear and confusing to what is meant by 'the first surface of the pillar is concentrically disposed within a surface area of the second surface of the pillar.' Where is this shown in the drawings of the elected species of figures 19A-19C? In claim 107 [sic], it is unclear and confusing to what is meant by 'the pillar is copper and has a conical shape, the first and second surfaces of the pillar are flat and parallel to one another and have a circular shape, and the first surface of the pillar is concentrically disposed within a surface area of the second surface of the pillar.' Where is this shown in the drawings of the elected species of figures 19A-19C?"

The limitations are clear and straightforward. Furthermore, the limitations are illustrated in the Drawings, as mentioned above. Unfortunately, the Examiner has not even attempted to explain what is unclear or confusing about these limitations.

Therefore, Applicant requests these rejections be withdrawn.

VII. SECTION 103 REJECTIONS – NAKATANI ET AL. AND LIN

Claims 1, 3-6, 8-11, 14, 16-18, 29-36, 101-105 and 109 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakatani et al.* (U.S. Patent No. 6,038,133) in view of *Lin* (U.S. Patent No. 6,402,970).

Nakatani et al.

Nakatani et al. discloses a circuit component built-in module.

The first embodiment describes circuit component built-in module 100 that includes insulating substrate 101, wiring patterns 102a and 102b, circuit components 103 and inner via 104. Insulating substrate 101 includes an inorganic filler and a thermosetting resin. Wiring patterns 102a and 102b are located on opposite surfaces of insulating substrate 101. Circuit components 103 include active component 103a (such as a semiconductor chip) and passive component 103b that are flip-chip bonded to wiring pattern 102b. Inner via 104 is a conductive resin that includes metal particles and a thermosetting resin.

The second embodiment describes a method for producing the circuit component built-in module. The materials and circuit components in the second embodiment are the same as those in the first embodiment.

The second embodiment includes forming sheet mixture 200 that includes an inorganic filler and a thermosetting resin (Fig. 2(a)), forming through-hole 201 in sheet mixture 200 using a laser, a drill or a mold (Fig. 2(b)), filling conductive resin composition 202 into through-hole 201 by screen printing (Fig. 2(c)), flip-chip bonding circuit component 204 to copper foil 203 using conductive resin 205 and optionally injecting a sealing resin between copper foil 203 and circuit component 204 (Fig. 2(d)), forming copper foil 206 (Fig. 2(e)), sandwiching sheet mixture 200 provided with conductive resin composition 202 between copper foil 203 provided with circuit component 204 and copper foil 206 (Fig. 2(f)), pressing sheet mixture 200 and copper foils 203 and 206 so that circuit component 204 is buried in sheet mixture 200 (Fig. 2(g)), curing sheet mixture 200 and conductive resin composition 202 and then etching or stamping copper foils 203 and 206 into wiring patterns 209 and 210 (Fig. 2(h)).

Sheet mixture 200 serves as insulating substrate 207, and conductive resin composition 202 serves as inner via 208 that electrically connects wiring patterns 209 and 210.

The third embodiment describes another method for producing the circuit component built-in module. The materials and circuit components in the third embodiment are the same as those in the first embodiment.

The third embodiment includes forming sheet mixture 300 that includes an inorganic filler and a thermosetting resin (Fig. 3(a)), forming through-hole 301 in sheet mixture 300 using a laser, a drill or a mold (Fig. 3(b)), filling conductive resin composition 302 into through-hole 301 by screen printing (Fig. 3(c)), forming wiring pattern 303 on release film 305 and then flip-chip bonding circuit component 304 to wiring pattern 303 using conductive resin and optionally injecting a sealing resin between wiring pattern 303 and circuit component 304 (Fig. 3(d)), forming wiring pattern 306 on release film 307 (Fig. 3(e)), sandwiching sheet mixture 300 provided with conductive resin composition 302 between release film 305 provided with wiring pattern 303 and with circuit component 304 and release film 307 provided with wiring pattern 306 (Fig. 3(f)), pressing sheet mixture 300 and release films 305 and 307 so that circuit component 304 is buried in sheet mixture 300 (Fig. 3(g)), curing sheet mixture 300 and conductive resin composition 302 and then peeling off release films 305 and 307 (Fig. 3(h)).

Sheet mixture 300 serves as insulating substrate 308, and conductive resin composition 302 serves as inner via 309 that electrically connects wiring patterns 303 and 306.

The fourth, fifth and sixth embodiments describe multilayered circuit component built-in modules based on the first, second and third embodiments, respectively.

Nakatani et al. is directed to a high density, high reliability module:

> It is the object of the present invention to provide a highly reliable circuit component build-in module in which circuit components are mounted with high density. (Column 1, lines 47-50.)

Nakatani et al. emphasizes forming the through-hole with a laser to obtain a high density, high reliability module:

> Laser processing is preferable because it allows formation of the through-hole 201 in a fine pitch and generates no debris. (Column 8, lines 64-66.)

Nakatani et al. also emphasizes forming the insulating substrate with a heat conductive inorganic filler to obtain a high reliability module:

> Furthermore, the first circuit component built-in module constitutes a highly reliable circuit component built-in module, because heat generated in the circuit components is released promptly by the inorganic filler. (Column 2, lines 4-7.)

Lin

Lin describes a support circuit that can be connected to a semiconductor chip to provide a semiconductor chip assembly.

Support circuit 48 is manufactured by providing copper foil 10 (Figs. 1A-3A), forming photoresist layers 16 and 18 on the top and bottom surfaces, respectively, of copper foil 10 (Figs. 1B-3B), patterning photoresist layers 16 and 18 to selectively expose the top and bottom surfaces, respectively, of copper foil 10 (Figs. 1C-3C), forming nickel etch masks 26 and 28 on the exposed portions of the top and bottom surfaces, respectively, of copper foil 10 (Figs. 1D-3D), stripping photoresist layers 16 and 18 (Figs. 1E-3E), etching partially through copper foil 10 from the top surface towards the bottom surface to form pillar 36 from an unetched portion of copper foil 10 protected by nickel etch mask 26 and recessed portion 38 from an unetched portion of copper foil 10 unprotected by nickel etch mask 26 (Figs. 1F-3F), forming insulative base 40 on the lower portion of pillar 36 and on recessed portion 38 (Figs. 1G-3G), etching completely through recessed portion 38 from the bottom surface towards the top surface to form routing line 42 from an unetched portion of recessed portion 38 protected by nickel etch mask 28 (Figs. 1H-3H), and stripping nickel etch masks 26 and 28 (Figs. 1I-3I).

The semiconductor chip assembly is manufactured by depositing adhesive 50 on the bottom surface of support circuit 48 and then mechanically attaching a semiconductor chip (not shown) to support circuit 48 using adhesive 50 (Figs. 1J-3J), and forming an opening in insulative base 40 by laser ablation to expose through-hole 44 in routing line 42 which in turn exposes a pad of the chip (Figs. 1K-3K). Thereafter, a connection joint can be formed in through-hole 44 that contacts and electrically connects routing line 42 and the pad.

Pillar 36 tapers inwardly with increasing height because the wet chemical etch undercuts (laterally etches) copper foil 10 beneath nickel etch mask 26.

Lin describes various advantages of the pillar:

> An advantage of the present invention is that the pillar is formed using etching (i.e., subtractively) rather than by electroplating or electroless plating (i.e., additively) which improves uniformity and reduces manufacturing time and cost. (Column 5, lines 4-7.)
>
> A pillar is particularly well-suited for reducing thermal mismatch related stress in the next level assembly. (Column 9, lines 65-67.)
>
> The tapered pillar yields enhanced reliability for the next level assembly that exceeds that of conventional BGA packages. (Column 11, lines 33-35.)

The Present Invention

Claim 1 recites "the pillar includes first and second opposing surfaces and tapered sidewalls therebetween." *Nakatani et al.* fails to teach or suggest that the inner via has tapered sidewalls. Instead, the inner via has vertical sidewalls.

Claim 1 also recites "the chip, the pillar and the encapsulant extend vertically beyond the routing line in the first direction." *Lin* fails to teach or suggest that the chip and the pillar extend vertically beyond the routing line in a first direction. Instead, the pillar extends vertically beyond the routing line in the first (upward) direction, and the chip is disposed vertically beyond the routing line in the second (downward) direction.

Furthermore, *Nakatani et al.* fails to teach or suggest a modification to *Lin* that provides the present invention, and likewise, *Lin* fails to teach or suggest a modification to *Nakatani et al.* that provides the present invention.

For example, the inner via in *Nakatani et al.* is formed additively whereas the pillar in *Lin* is formed subtractively. Therefore, the inner via is not interchangeable with the pillar.

As another example, the wiring pattern and the inner via in *Nakatani et al.* are attached to one another whereas the routing line and the pillar in *Lin* are integral with one another. Therefore, the wiring pattern and the inner via are not interchangeable with the routing line and the pillar.

As another example, the inner via extends across the chip thickness in *Nakatani et al.* whereas the pillar extends across none of the chip thickness in *Lin*. Therefore, the vertical position of the inner via relative to the chip is not interchangeable with that of the pillar relative to the chip.

Nakatani et al. and *Lin* disclose completely different semiconductor packages and methods of manufacture. Little or nothing in one is applicable to the other. Moreover, *Nakatani et al.* cannot be modified in view of *Lin* or vice-versa to provide the present invention.

The Rejection

In sustaining this rejection, the Examiner asserts "Therefore, it would have been obvious to one of ordinary skill in the art to use Lin's pillar shape to modify Nakatani et al.'s pillar shape for the purpose [of] reducing stress and improving reliability."

The Examiner's position, as best Applicant understands, is that neither *Nakatani et al.* nor *Lin* , alone or in combination, teach or suggest forming the through-hole (and thus the inner via) with tapered sidewalls, but one of ordinary skill in the art would be motivated to do so in order to reduce stress and improve reliability.

The rejection is flawed for several reasons.

First, the proposed modification would not reduce stress. *Nakatani et al.* makes clear that the inner via is buried between the wiring patterns and sealed in the heat conductive insulating substrate that is thermally matched to the chip. Therefore, the inner via with tapered sidewalls would have little or no effect on thermal stress. In *Lin* the pillar is a dangling lead that interfaces with an external component in the next level assembly, and therefore the tapered sidewalls provide a larger internal surface at a high stress region.

Second, the proposed modification would degrade reliability. *Nakatani et al.* makes clear that preferably laser processing forms the through-hole because it generates no debris. However, laser processing could not form the through-hole with tapered sidewalls. Therefore, forming the through-hole with tapered sidewalls would generate more debris. *Nakatani et al.* also makes clear that the conductive resin composition is deposited by screen printing and fills the through-hole so that the inner via contacts the wiring patterns. However, the through-hole with tapered sidewalls where diameter increases as depth increases would be more difficult to fill by screen printing.

Third, the proposed modification would degrade density. *Nakatani et al.* makes clear that preferably laser processing forms the through-hole because it provides fine pitch. However, laser processing could not form the through-hole with tapered sidewalls. Therefore, the through-hole with tapered sidewalls would have larger pitch. *Nakatani et al.* also makes clear that the through-hole extends across the thickness of the chip. However, the through-hole with tapered sidewalls would be wider and would need to be laterally shifted away from the chip to maintain proper spacing, thereby enlarging the module. In *Lin* the pillar is vertically offset from the chip and therefore the tapered sidewalls do not enlarge the support circuit.

Thus, the proposed modification is contrary to the stated objectives of providing a high density, high reliability module, results in numerous disadvantages with no apparent advantages and would render the module unsatisfactory for its intended purpose. As a result, one skilled in the art would have absolutely no motivation to make the proposed modification. Moreover, in the absence of any teaching, suggestion or motivation, the proposed modification is nothing more than hindsight reconstruction based on the present application.

Claims 9 and 104 recite "the pillar is copper." *Nakatani et al.* fails to teach or suggest that the inner via is copper. Instead, the inner via is a thermosetting conductive substance that includes a thermosetting resin such as epoxy resin, phenol resin or cyanate resin. In sustaining these rejections, the Examiner merely parrots the cited claim language without any attempt to explain how it reads on *Nakatani et al.*

Claim 29 recites "an insulative base that contacts the routing line, and extends vertically beyond the chip, the routing line and the pillar in the second direction." *Nakatani et al.* fails to teach or suggest the insulative base. In sustaining this rejection, the Examiner asserts that *Nakatani et al.* includes "routing line 303" and "encapsulant 308" and the insulative base is the "lower portion of 308." This is clearly erroneous. The encapsulant and the insulative base cannot be construed as "portions" of insulating substrate 308. Instead, the encapsulant and the insulative base are separate features. Furthermore, insulating substrate 308 does not extend vertically beyond wiring pattern 303 in the second (downward) direction.

Claim 33 recites "the adhesive contacts and is sandwiched between the routing line and the pad." *Nakatani et al.* fails to teach or suggest the adhesive. In sustaining this rejection, the Examiner asserts that *Nakatani et al.* includes "chip 304" and "encapsulant 308" and "insulative adhesive 308." This is clearly erroneous. The encapsulant and the adhesive cannot both be construed as insulating substrate 308. Instead, the encapsulant and the adhesive are separate features. Furthermore, insulating substrate 308 does not contact the pad on circuit component 304.

Claim 35 recites "a second terminal that contacts the routing line, extends vertically beyond the routing line in the second direction." *Nakatani et al.* fails to teach or suggest the second terminal. In sustaining this rejection, the Examiner asserts that *Nakatani et al.* includes "routing line 303" and "second terminal 306." This is clearly erroneous. Wiring pattern 306 does not contact wiring pattern 303 and does not extend vertically beyond wiring pattern 303 in the second (downward) direction.

Claim 36 recites "a first terminal that is plated on the first surface of the pillar, extends vertically beyond the pillar in the first direction and is spaced from the connection joint, and a

second terminal that is plated on the routing line, extends vertically beyond the routing line in the second direction and is spaced from the connection joint and the first terminal." *Nakatani et al.* fails to teach or suggest the first terminal or the second terminal. In sustaining this rejection, the Examiner asserts that *Nakatani et al.* includes "routing line 303" and "first terminal 303" and "second terminal 306" and "pillar 309." This is clearly erroneous. Wiring pattern 303 is not plated on inner via 309 and does not extend vertically beyond inner via 309 in the first (upward) direction, and wiring pattern 303 is not plated on itself and does not extend vertically beyond itself in the second (downward) direction.

To establish prima facie obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. See M.P.E.P. § 2142.

It is insufficient that the prior art shows similar components unless it also contains some teaching, suggestion or incentive for arriving at the claimed structure. See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990).

Moreover, if the proposed modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. See M.P.E.P. § 2143.01.

Nakatani et al. fails to teach or suggest independent claims 1 and 21 as well as numerous rejected dependent claims, and *Lin* fails to cure these deficiencies. Therefore, Applicant requests that these rejections be withdrawn.

VIII. SECTION 103 REJECTION – NAKATANI ET AL., LIN AND FUJITSU

Claim 22 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakatani et al.* in view of *Lin* and further in view of *Fujitsu* (U.S. Patent No. 5,654,584).

Fujitsu discloses a semiconductor device that includes semiconductor chip 11, epoxy adhesive 16, TAB tape 17 and metal plating layer 20. Semiconductor device 11 includes electrode pad 14, and TAB tape 17 includes organic film material 18 and inner lead 19.

Semiconductor chip 11 is adhered to TAB tape 17 by epoxy adhesive 16, and electrode pad 14 is electrically connected to inner lead 19 by metal plating layer 20.

Claim 22 recites "the connection joint is an electrolessly plated metal ." *Nakatani et al.* fails to teach or suggest that the circuit component is flip-chip bonded to the wiring pattern by electrolessly plated metal. Instead, the circuit component is flip-chip bonded to the wiring pattern by gold, solder or conductive adhesive. *Fujitsu* fails to teach or suggest that the semiconductor chip is flip-chip bonded to the inner lead. Instead, the semiconductor chip is TAB bonded to the inner lead.

In sustaining this rejection, the Examiner admits that "Fujitsu [discloses] tape automated bonding leads" but asserts "Therefore, it would have been obvious to one of ordinary skill in the art to use Fujitsu's plated metal connection joint to modify the combination of Nakatani et al. and Lin's connection joint for the purpose of preventing damage to the semiconductor chip under the electrode pad."

The Examiner's position is vague and confusing. The Examiner does not even attempt to explain "the combination of Nakatani et al. and Lin's connection joint." Applicant need not second-guess what this connection joint is.

Furthermore, the metal plating layer in *Fujitsu* is inapplicable to the flip-chip bond in *Nakatani et al.*

Therefore, Applicant requests that this rejection be withdrawn.

IX. NEW CLAIMS

Claims 111-115 have been added to further explicate various features of the invention. No new matter has been added.

Claim 111 recites "the pillar is metal." *Nakatani et al.* fails to teach or suggest this approach, as mentioned above for claims 9 and 104.

Claim 112 recites "the pillar is a single-piece metal." *Nakatani et al.* fails to teach or suggest this approach, as mentioned above for claims 9 and 104.

Claim 113 recites "the pillar is formed subtractively." *Nakatani et al.* fails to teach or suggest this approach. Instead, the inner via is formed additively.

Claim 114 recites "the first surface of the pillar contacts a terminal at an electroplated interface between different metals." *Nakatani et al.* fails to teach or suggest this approach. Instead, the conductive resin composition contacts the top wiring pattern and then is cured to form the inner via.

Claim 115 recites "the second surface of the pillar contacts the routing line at an electroplated interface between different metals." *Nakatani et al.* fails to teach or suggest this approach. Instead, the conductive resin composition contacts the bottom wiring pattern and then is cured to form the inner via.

X. FEES

The fee for additional claims 111-115 is calculated below:

For	Claims Remaining After Amendment	Highest Number Previously Paid For		Extra Claims	Rate		Additional Fee
Total Claims	190	– 160	=	30	x 25	=	$750
Independent Claims	6	– 6	=	0	x $100	=	$0
Multiple Dep. Claim	1	1	=	0	x $180	=	$0
Total Fee						=	$750

Please charge the $750 to Deposit Account No. 502178/BDG024 and charge any underpayment or credit any overpayment to this Account.

XI. CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 18, 2005

D Sigmond — 11/18/05

David M. Sigmond — Date of Signature
Attorney for Applicant

Respectfully submitted,

D Sigmond

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